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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,386	06/19/2001	Son H. Lam	219.40057X00	1333

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Schwegman, Lundberg, Woessner & Kluth P.A.
c/o Anne Richards
1600 TCF Tower
121 S. 8th Street
Minneapolis, MN 55402

EXAMINER	
ELAMIN, ABDELMONIEM I	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,386	LAM, SON H.	
	Examiner	Art Unit	
	A Elamin	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. *Claim 6-9, 11-16*, are rejected under 35 U.S.C. 102(e) as being anticipated by Green, US. Pat. No. 6,496,881.

3. Claim *6*, Green teaches an apparatus for fault resilient booting [*title, abstract*], comprising:

a first processor designated as a bootstrap processor [*col. 3, lines 13-16*];

a latch for turning off said bootstrap processor [*abstract, Fig. 2, col. 3, lines 19-23*];

a control unit [*control logic 64 of Fig. 2*] for providing control signals for setting said latch, for resetting said latch and for controlling additional processors [*col. 5, line 55 thru col. 6, line 5*].

4. Claims *7, 8, 12*, Green teaches a timer providing a signal indicating that a predetermined time has expired, which is applied to said latch to set said latch [*timer 71 of Fig. 2*];

said control unit providing a first signal to said latch for setting said latch, a second signal applied to said latch for resetting said latch, a third signal for controlling other processors and a fourth signal for resetting the timer [*timer 71 of Fig. 2 and related disclosure*].

5. Claim *9*, Green teaches the bootstrap processor is considered to fail if said timer is not reset before reaching said predetermined time [*col. 3, lines 19-23*].

6. Claims *11, 15*, Green teaches the apparatus is part of an appliance server management system [*col. 4, lines 16-23*].

7. Claims *13-14*, Green teaches said first signal from said control unit is generated when said bootstrap processor fails a power-on self-test or a built-in self-test [*abstract, col. 3, lines 4-45*].

8. Claim *16*, Green teaches said control unit causes another processor to become the bootstrap processor when said bootstrap processor is disabled by said latch [*col. 3, lines 4-45*].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim *10* are rejected under 35 U.S.C. 103(a) as being unpatentable over Green, US. Pat. No. 6,496,881.

11. Claim *10*, Green fails to teach said control unit includes a system I/O chip.

Official notice is taken that both the concept and the advantages of I/O chip is old and well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Green to include an I/O chip, because it provides I/O terminals and control

logic for commonly used legacy peripheral devices such as keyboards, IDE drives, IEEE parallel ports, serial communication ports.

12. Claims *1-5* are rejected under 35 U.S.C. 103(a) as being unpatentable over Natu, US. Pat. No. 5, 5,790,850 (*previously cited*) in view of Green, US. Pat. No. 6,496,881.

13. Claim *1*, Natu teaches a method of a fault resilient booting in a multiprocessor system [*title, abstract*], comprising:

designating one processor as a bootstrap processor [*Step 110 of Fig. 2A, col. 3, lines 44-45*];

testing the bootstrap processor to verify that it will run BIOS code [*col. 3, lines 48-51*];

testing during a POST the operation of said bootstrap processor [*Fig. 2A, col. 3, lines 44-50*];

testing during BIST the operation of said bootstrap processor [*Fig. 2A, col. 3, lines 54-57*];

assigning the bootstrap process to another processor if said bootstrap processor fails a test [*Fig. 2A, col. 3, lines 60-62*];

said steps being implemented in an appliance server management system [*title, abstract*].

Natu fails to teach setting a latch for disabling said bootstrap processor if the testing indicates failure.

Green teaches a system for assigning bootstrap processor in a multiprocessor computer [*title, abstract*], comprising setting a latch for disabling bootstrap processor if the testing indicates failure [*abstract, col. 3, lines 4-45*].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Natu to include setting a latch for disabling bootstrap processor if the testing indicates failure, because if the failing processor has internal failure, it may not be able to operate properly to remove itself from the operation. Thus disabling the failing processor eliminates the problem of relying on a failing processor to perform the appropriate action to remove itself from operation [*see Green, col. 2, lines 58-68*].

14. Claim *2*, Green teaches a timer which indicates a failure if the bootstrap processor is not reset within a predetermined period [*timer 71 of Fig. 2*].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Natu to include a timer which indicates a failure if the bootstrap processor is not reset within a predetermined period, because it indicates unsuccessful bootstrapping and hence, the system will initiate a second reset operation and assign the bootstrapping function to another processor [*col. 3, lines 4-45*].

15. Claim *3*, Natu teaches failure in the second or third testing step also causes said latch to be set [*see Natu, Figs. 2A, 2B and related disclosure*].

16. Claims *4-5*, Natu teaches the testing steps are controlled by a controller [*see Natu, abstract*].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A Elamin whose telephone number is (571) 272-3674. The examiner can normally be reached on MON-FRI 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A Elamin
Primary Examiner
Art Unit 2116

September 15, 2005